Microcontrollers Final Project Proposal

John Call, Ray Elison, Landon Wilcox

For our final project we propose to implement a hardware-level internet filter. The microcontroller will be connected to two Ethernet chips, in between a single computer and a network router. We propose to use the Wiz550io chip (http://www.wiznet.co.kr/product-item/wiz550io/) to interface with. We believe we can configure it to abstract out the lower-level Ethernet frames and provide us with the data frame normally sent to the computer over an SPI interface.

When the computer sends out a request for "bing.com" our microcontroller will reply with an appropriate packet to display a page indicating the request was blocked. Other communications will be forwarded to the second Ethernet interface, and all incoming transmissions will pass through.

Alternative design options considered include: filtering on incoming traffic and sending a reset signal to the router on blocked traffic, sending a reset signal to the computer so a web browser will render a "request timed out" page specific to the browser, using a smaller chip (the Wiz820io, am not sure how much configuration either chip would require relative to the other, or how much of the OSI it would abstract for us).